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Direct Observation of Loadlines in MESFET by Using Average RF Gate and Drain Currents

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ABSTRACT — **A device at a given bias point can experience different gain compression mechanisms for different loadline impedances. The observation of loadline impedance for power MESFETs using experimental average rf gate and drain currents at 1dB gain compression point is demonstrated in this paper. We found that there is a distinct signature in average rf gate and drain currents to characterize each gain compression mechanism. By using this novel method, circuit optimization of power amplifiers can be easily achieved.**

I. INTRODUCTION

It is often desirable to have some methods to experimentally observe loadline impedance presented to the device for MMIC or hybrid amplifiers. A device at one given bias point may have different gain compression mechanisms for various loadline impedances. Knee voltage, pinch-off voltage, breakdown voltage and maximum drain current clip output I-V waveform of a power MESFET and cause gain compression. The exact loadline impedance does not affect gain compression mechanism when a device is biased very close to the gain compression region. Meng et al [1] used a simple maximum Psat load pull condition and biased the MESFET device adjacent to each gain compression region. It was shown that each clipping mechanism has its distinct signature in average rf gate and drain currents [1]. However, the gain compression mechanism is very sensitive to the loadline impedance presented to the device at a normal biased point. A power MESFET device is normally biased at 50% Idss (class A) for linearity and below 25% Idss (class AB) for efficiency.

Cripps [2] pointed out that the constant P_{1dB} contour of a power MESFET has a near elliptical shape in the Smith Chart. The two impedances along the short axis in an oval-shaped constant P_{1dB} contour correspond to pure real load resistance —R_{LO} and R_{HI}. The impedance of the maximum P_{1dB} is R_{opt} and R_{LO} (R_{HI}) has impedance less (higher) than R_{opt}. Large signal performances as a function of input power are measured at various R_{LO} and R_{HI} impedances for a given bias point. R_{LO} and R_{HI} have very distinct difference in average rf gate and drain currents at P_{1dB}. Thus, the observation of R_{LO} and R_{HI} under load-pull condition for power MESFETs using experimental average rf gate and drain currents at 1dB gain compression point is demonstrated in this paper. Neighboring bias points with the same gate voltage or the same drain voltage can be used to estimate and even determine R_{LO} and R_{HI}.

II. DEVICE STRUCTURE AND DC CHARACTERISTICS

A GaAs MESFET device with doping density of $2.6x10^{17}/cm^3$ and 1 μm gate length is used to study gain compression mechanisms at different bias points. The fabricated device has 1.5 V knee voltage, 200 mA/mm Idss, -2V pinch-off voltage and 14V gate-to-drain breakdown voltage. Figure 1 illustrates the I-V curve of the device withgate width of 6X50 μm.

The purpose of this paper is to observe loadline by using average rf gate and drain currents for MESFETs under load-pull condition. Thus, five bias points were chosen and are illustrated in figure 1. These five bias points are: a close-to-optimum bias point (equally away from all the gain compression mechanisms) at Vds=7 V and Vgs=-1V, the bias point toward knee voltage (Vds=4V and Vgs=-1V), the bias point toward breakdown voltage (Vds=10V and Vgs=-1V), the bias point toward maximum drain current (Vds=7V and Vgs=-0.5 V) and the bias point toward pinched-off region (Vds=7V and Vgs=-1.5V). Two bias points have the same gate voltage as the close-to-optimum bias point; while the other two bias points have the same drain voltage as the close-to-optimum bias point.

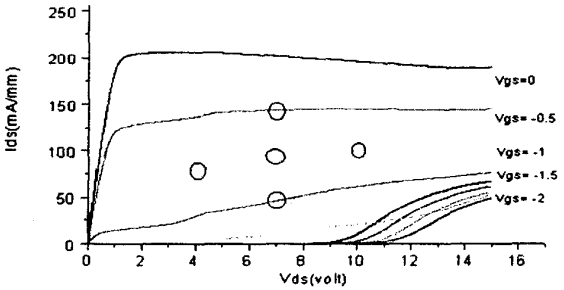

Fig. 1 The five bias points and device I-V curve.

A commercial ATN load pull system is used here to acquire experimental data. The measured coplanar devices have gate width of 6X50 μm. A CW signal ranging from –20dBm to +7dBm at a fixed frequency of 1.8 GHz is applied to the device in the load pull measurement. The input tuner impedance is set to maximize small signal gain

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while the output tuner impedance is set at various load impedances in the Smith Chart. Large signal performances as a function of input power are then measured at various load impedances for each bias point. Figure 2 illustrates the typical experimental constant power contour from load-pull measurement when input power is set at 0 dBm.

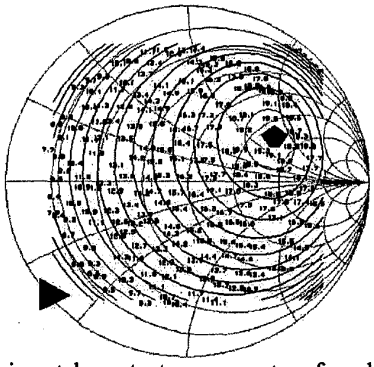

Fig. 2 Experimental constant power contour from load-pull

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

There are eight situations for the four neighboring biasing points because each bias point has R_{LO} and R_{HI} cases. Four out of eight situations are simple and discussed first.

It can be easily understood that the gain compression mechanism is the knee voltage for bias point toward knee voltage with R_{HI} load impedance. Figure 3 illustrates output power, the average rf gate and drain current as a function of input power at Vds=4V Vgs=-1V (bias toward knee voltage) with R_{HI} load impedance. The average rf gate current is zero and average drain current remains unchanged when gain compression (near P_{1dB}) occurs. In other words, gate is not strongly forward-biased when knee voltage clips output waveform.

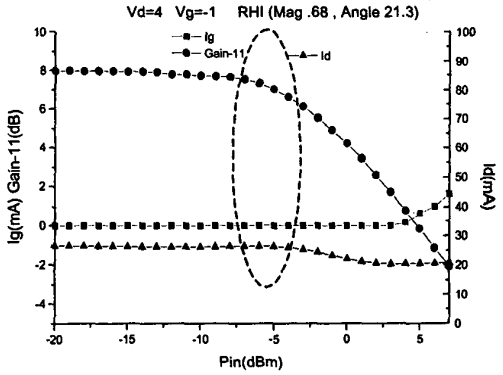

Fig. 3 Gain, I_g and I_d vs. P_{in} when biased toward knee voltage with R_{HI} load impedance. The corresponding gain compression mechanism is the knee voltage (I_g=0 and I_d unchanged at G_{1dB}).

It is straightforward that the gain compression mechanism is the pinch-off voltage for bias point toward pinch-off voltage with R_{LO} load impedance. The power performance and average rf currents when biased at Vds=7V Vgs=-1.5V (bias toward pinch-off voltage) with R_{LO} load impedance are illustrated in figure 4. The operation changes from class A to class AB as input signal becomes larger [2]. Thus, the average drain current increases at P_{1dB}. However, gate current is zero because gate is still in reverse bias condition when gain compression occurs.

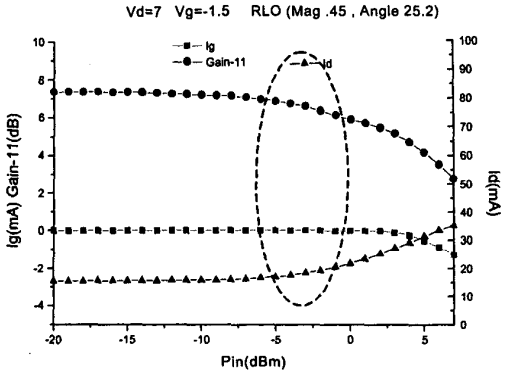

Fig. 4 Gain, I_g and I_d vs. P_{in} when biased toward pinch-off voltage with R_{LO} load impedance. The corresponding gain compression mechanism is the pinch-off voltage (I_g=0 and I_d increasing at G_{1dB}).

It is obvious that the gain compression mechanism is the breakdown voltage for bias point toward breakdown voltage with R_{HI} load impedance. Breakdown voltage can also cause gain compression and the case is illustrated in figure 5 for Vds=10V Vgs=-1V (bias toward breakdown voltage) with R_{HI} load impedance. The average rf gate current becomes negative and the average rf drain current increases near P_{1dB}. The increase in drain current comes from the generation of positive drain current by avalanche breakdown at large drain voltage swing. Also, there exists negative gate current flowing into the gate when the large drain voltage swing reaches breakdown voltage.

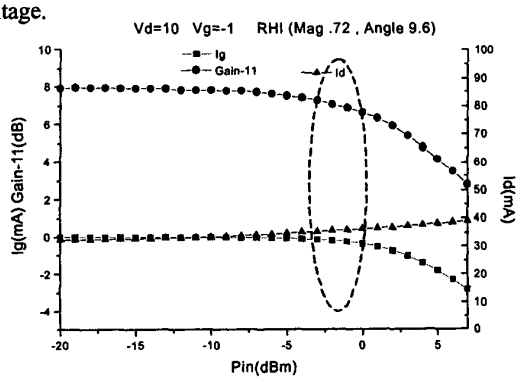

Fig. 5 Gain, I_g and I_d vs. P_{in} when biased toward breakdown voltage with R_{HI} load impedance. The corresponding gain compression mechanism is the breakdown voltage (I_g<0 and I_d increasing near G_{1dB}).

It can be observed easily that the gain compression mechanism is the maximum drain current for bias point toward maximum drain current with R_{LO} load impedance. Figure 6 illustrates power performance and the average rf current when Vds=7V Vgs=-0.5V (bias toward maximum drain current) with R_{LO} load impedance. The average rf gate current is positive when gain compression (near P_{1dB}) occurs. The average drain increase slightly and then flattens out when input power increases because the higher transconductance near maximum drain current tends to increase the rf drain current while the current clipping effect caused by the maximum drain current tends to decrease the rf drain current. The current clipping effect caused by maximum drain current is further complicated by the gate contour and has been discussed by Meng et al [1]. The average rf drain current tends to decrease more in the wide-recessed device than in the narrow recessed-device when gain compression caused by maximum drain current occurs. This effect can be explained by the fact that surface depletion caused by the Fermi level pinning blocks current conduction for the case of a wide-recessed structure and thus reduces maximum rf drain current when gate is at its forward rf swing. Thus, the corresponding gain compression mechanism in figure 6 is the maximum drain current.

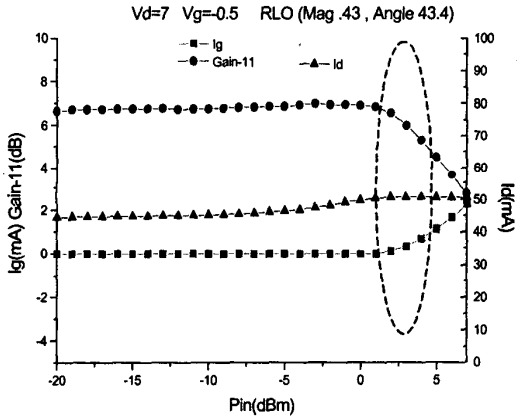

Fig. 6 Gain, I_g and I_d vs. P_{in} when biased toward maximum drain current with R_{LO} load impedance. The corresponding gain compression mechanism is the maximum drain current (I_g>0).

The gain compression mechanism for other four situations of neighboring bias points depends on the magnitude of load resistance. Take the bias point toward breakdown voltage as an example. Figure 7 and figure 8 correspond to power performance of two different R_{LO}. The load resistance in figure 7 is larger because the corresponding reflection coefficient in the Smith chart is closer to the center of constant power contour (R_{opt} point). Thus, it can be observed that the gain compression mechanism in figure 7 is the breakdown voltage; while the gain compression mechanism in figure 8 is the pinch-off voltage.

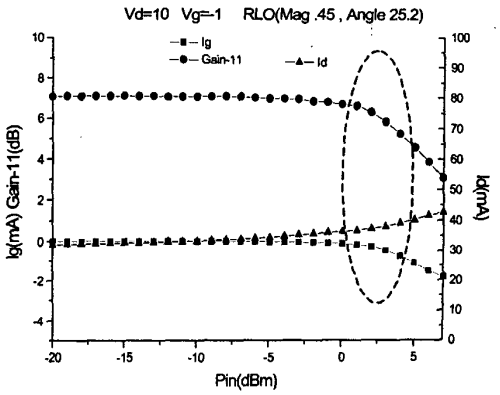

Fig. 7 Gain, I_g and I_d vs. P_{in} when biased toward breakdown voltage with R_{LO} load impedance. The corresponding gain compression mechanism is the breakdown voltage (I_g<0 and I_d increasing at G_{1dB}).

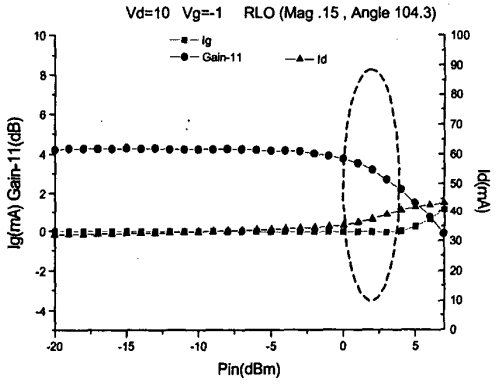

Fig. 8 Gain, I_g and I_d vs. P_{in} when biased toward breakdown voltage with R_{LO} load impedance. The load impedance is smaller than that in figure 7. The corresponding gain compression mechanism is the pinched-off voltage (I_g=0 and Id increasing at G_{1dB}).

Figure 9 corresponds to the power performance of R_{HI} at the close-to-optimum bias point. It can be observed from average rf gate and drain currents near P_{1dB} that the gain compression mechanism in figure 9 is the mixing combinations between breakdown voltage and knee voltage. The device experiences the knee gain compression mechanism slightly earlier than the breakdown gain compression mechanism as revealed in figure 9. The power performance of R_{LO} at the close-to-optimum bias point is illustrated in figure 10. Certainly, figure 10 corresponds to the mixing combinations between pinch-off voltage and maximum drain current as observed from average rf gate and drain current near P_{1dB}. The pinch-off voltage gain

compression mechanism occurs slightly earlier than the maximum drain current gain compression mechanism as revealed in figure 10. It is also worthwhile to be mentioned that the linear gain in figure 9 is 3.5 dB higher than that in figure 10 because the R_{HI} is closed to the impedance of maximum gain matching condition.

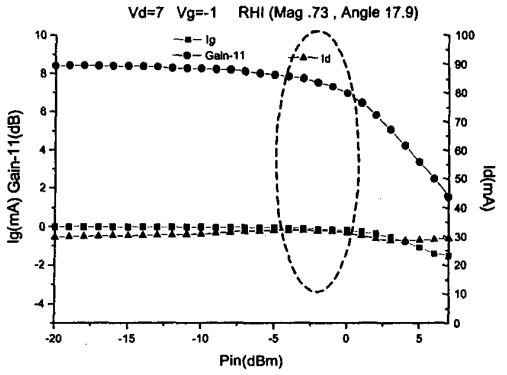

Fig. 9 Gain, I_g and I_d vs. P_{in} when biased close to optimum bias point with R_{HI} load impedance. The gain compression mechanism is the mixing combination between knee voltage and breakdown voltage as shown at I_g and I_d when G_{1dB} occurs.

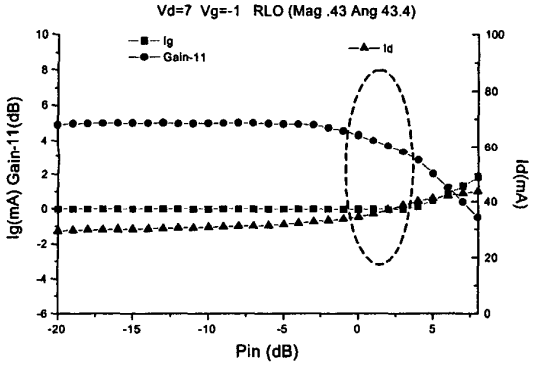

Fig. 10 Gain, I_g and I_d vs. P_{in} when biased close to optimum bias point with R_{LO} load impedance. The gain compression mechanism is the mixing combination between maximum drain current and pinched-off voltage as shown at I_g and I_d when G_{1dB} occurs.

IV. CONCLUSION

The gain compression mechanism is very sensitive to the loadline impedance presented to the device at normal biased points. Knee voltage, pinch-off voltage, breakdown voltage and maximum drain current clip output I-V waveform of a power MESFET and cause gain compression. It was shown that each clipping mechanism has its distinct signature in average rf gate and drain currents near P_{1dB}. The loadline impedance can thus be found through identifying gain compression signatures at its bias point and the neighboring bias points. In summary, the observation of loadline impedance for power MESFETs using experimental average rf gate and drain currents at 1dB gain compression point is demonstrated.

ACKNOWLEDGEMENT

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